REMARKS

Claims 1-2, 4-6 and 21-22 are pending in the Application. Claims 1, 4 and 5 have been amended. Claims 3 and 7-20 have been canceled without prejudice. Claims 21 and 22 have been added; however, no additional claims fees are required.

Election/Restriction

The Patent Office required restriction between Group I, Claims 1-6 and 19-20 and Group II, Claims 7-18.

Applicant affirms election of Group I, Claims 1-6 and 19-20 with traverse.

Claim Objections

The Patent Office objected to claim 14 for informalities.

Claim 14 has been canceled without prejudice, thus the objection is now moot.

Claim Rejections – 35 USC § 103

The Patent Office rejected claims 1-6 and 19-20 under 35 U.S.C. § 103(a) as being unpatentable over Forbes, U. S. Patent No. 6,201,287 (Forbes) in view of Gagne et al., U.S. Patent No. 6,385,019 (Gagne) and further in view of Grzegorek, U.S. Patent No. 5,760,456 (Grzegorek).

Applicant respectfully traverses. Applicant respectfully submits claim 1 includes novel and nonobvious elements. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In reRyoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970). Applicant respectfully submits claim 1 recites elements which have not been disclosed, taught or suggested by Forbes, Gagne and Grzegorek, individually or in combination. For example, claim 1 generally recites circuitry for generating a negative capacitance, the circuitry comprising at least two transistors; at least two resistors; each resistor of said at least two resistors being coupled to each of

said at least two transistors; and a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

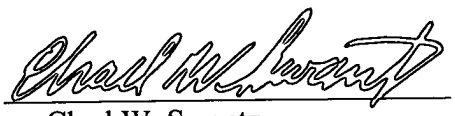
Forbes, Gagne and Grzegorek fail to disclose, teach or suggest circuitry for generating a negative capacitance, the circuitry comprising at least two transistors; at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors; and a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors. The Patent Office is correct in its statement that Forbes fails to disclose circuitry for generating a negative capacitance as recited in claim 1. However, Gagne fails to cure the defects of Forbes. The Patent Office cites FIG. 3a of Gagne for support of its assertion. FIG. 3a of Gagne discloses amplifiers A1 and A3. (Gagne, Column 3, Lines 40-50). An amplifier is not equivalent to a transistor as recited in claim 1. Additionally, claim 1 recites each resistor of said at least two resistors being coupled to each of said at least two transistors. Emphasis added. The Patent Office points to resistors R1 and Rm1 for support of its assertion. However, resistor R1 is only coupled to one amplifier (amplifier A3) and is not coupled to amplifier A1. Resistor Rm1 is also only coupled to one amplifier (amplifier A1) and is not coupled to amplifier A3. Thus, Gagne does not disclose each resistor of said at least two resistors being coupled to each of said at least two transistors. Consequently, elements of claim 1 have not been disclosed, taught or suggested by Forbes, Gagne and Grzegorek. Consequently, under *in re Ryoka*, claim 1 should be allowed. Claims 2 and 4-6 are allowable for being dependent upon an allowable base claim. Claims 21 and 22 are believed allowable for similar rationale as claim 1.

CONCLUSION

In light of the foregoing argument, reconsideration of all pending claims is requested, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,
LSI Logic, Inc.,

Dated: January 3, 2006

By: 
Chad W. Swantz
Reg. No. 46,329

SUITER · WEST· SWANTZ PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile